

REMARKS

I. Rejections Under 35 U.S.C. § 102(e)

Claims 1-6 were rejected by the Examiner under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,656,785 to Chiang et al., hereinafter referred to as "Chiang". The Examiner argued that Chiang, in col. 2, lines 34-37, in col. 3, lines 1-36, in col. 4, lines 59-67, in col. 6, lines 9-15, discloses a process for forming a low-temperature MIM capacitor that integrates a copper layer as the metal layer, said process comprising an MIM capacitor on a substrate, depositing a copper layer on the substrate to form the metal layer of the MIM capacitor, wherein the MIM capacitor is used for logic-based embedded DRAM devices (claims 1-2 and 18-19).

The Examiner further asserted that Chiang, in col. 6, lines 29-30, and in col. 7, lines 38-40, discloses that a photoresist layer (DRAM crown) is deposited on the layers of the substrate so as to enable DRAM crown lithography (claims 3 and 20). The Examiner also argued that Chiang, in col. 5, lines 1-13, in col. 6, lines 1-8, discloses the MIM capacitor formation process including a) forming transistors during an FEOL process, b) forming an interlayer dielectric layer, c) forming an HAR contact on the substrate, and d) forming a W-plug on the substrate (claims 4 and 21).

The Examiner additionally argued that Chiang, in col. 6, lines 1-18, in col. 7, lines 1-49, in col. 11, lines 1-14, discloses depositing a metal-1 oxide layer performing photo and etch operations on the deposited layers of the substrate, depositing copper and/or Ta layer, and performing a CMP process on the substrate (claims 5 and 22). The Examiner additionally argued that Chiang, in col. 9, lines 1-39, discloses the deposition of a metal-2 oxide layer, followed by a VIA-1 photo and etch process (DRAM photo and etch) (claims 6 and 23).

The Applicants respectfully disagree with this assessment. Applicants' amended claim 1 is directed toward a method for integrating copper with an MIM

capacitor during the formation the MIM capacitor, the method comprising the steps of: forming an MIM capacitor upon a substrate for use with an embedded DRAM; and depositing at least one copper layer upon the substrate and layers thereof to form at least one metal layer from which the MIM capacitor is formed, wherein the at least one copper layer, the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device. Similarly, Applicants' amended claim 18 teaches an MIM capacitor which integrates copper deposition during the formation of the MIM capacitor, the MIM capacitor comprising: an MIM capacitor formed upon a substrate for use with an embedded DRAM; and at least one copper layer deposited upon the substrate and layers thereof to form at least one metal layer from which the MIM capacitor is formed, wherein the at least one copper layer, the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device.

Applicants note that in both amended claims 1 and 18, Applicants disclose that the copper layer (i.e., one or more copper layers), the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device. Dependent claims associated with claims 1 and 18 further clarify this particular aspect of amended claims 1 and 18. Thus, the Applicants believe that the Examiner's arguments presented above in support of the rejection to claims 1-6 under 35 U.S.C. § 102(e) as being anticipated by Chiang are moot in light of the fact that Chiang does not teach, disclose or suggest that the copper layer (i.e., one or more copper layers), the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device.

Applicants remind the Examiner that in order to succeed in setting forth a rejection under 35 U.S.C. § 102(e) based on a particular reference, the reference cited must disclose ALL of the steps and/or features of the rejected claims. If even one feature or step is lacking in the cited reference, then the rejection under 35 U.S.C. § 102(e) must be withdrawn. In the present case, Chiang does not teach, disclose or suggest that the copper layer (i.e., one or more copper layers), the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device. Therefore, Applicants believe that the aforementioned rejection under 35 U.S.C. § 102(e) has been traversed. Applicants thus request that the aforementioned rejection under 35 U.S.C. § 102(e) be withdrawn.

II. Rejections Under 35 U.S.C. § 103(a)

Claims 16-17 and 33-34 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,656,785 (i.e., Chiang) in view of U.S. Patent No. 6,271,084 to Tu et al, hereinafter referred to as "Tu". The Examiner referred to the rejection under 35 U.S.C. § 102(e) with respect to Chiang in support of the rejection to claims 16-17 and 33-34 under 35 U.S.C. § 103(a). The Examiner argued that the difference between the claims and Chiang is that Chiang does not disclose forming the MIM capacitor utilizing at least one black diamond layer, wherein the diamond layer possesses a low K value permitting an associated AC delay to be reduced with increasing associated speeds thereof (claims 16 and 33). The Examiner also admitted that Chiang does not disclose forming the black diamond layer above an SiC layer and forming an SiON layer above the diamond layer (claims 17 and 34).

The Examiner asserted, however, that Tu, in Col. 2, lines 40-46, in col. 3, lines 14-27, discloses that a first insulator stop layer is formed followed by the deposition of a low K dielectric layer such as black diamond layers and then a

second insulator stop layer is deposited on the diamond layer wherein the first and second insulator stop layer comprise SiON or SiC layers.

The Examiner therefore argued that it would have been obvious to a skilled artisan to modify Chiang by employing the method of depositing low k dielectric layers to form MIM capacitors as taught by Tu because Tu, in col. 1, lines 52-67, and in col. 2, lines 1-14, and in col. 4, lines 53-67, discloses that the low K dielectric layer is used for forming the dual damascene opening and the dual damascene process enables a reduction in the topology created by DRAM capacitor structures.

The Applicants respectfully disagree with this assessment. Applicants' amended claims 1 and 18, upon which claims 16-17 and 33-34 respectfully depend teaches that the copper layer (i.e., one or more copper layers), the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device. Applicants therefore submit that the Examiner's arguments with respect to the rejection to claims 16-17 and 33-34 are moot in light of the fact that claims 1, 16-17 and 18, 33-34 do not teach that that the copper layer (i.e., one or more copper layers), the substrate and layers thereof are subject to a TaN sputter deposition process following by photoresist and coating operations for forming at least one recess within the embedded DRAM device.

The Applicants also remind the Examiner that the language of the references may not taken out of context and combined them without motivation, in effect producing the words of the claims (and sometimes, not even the words or concepts of the claims), without their meaning or context. The resultant combination would not yield the invention as claimed. The claims are rejected under 35 U.S.C. §103(a) and no showing has been made to provide the motivation as to why one of skill in the art would be motivated to make such a combination, and further fails to

provide the teachings necessary to fill the gaps in these references in order to yield the invention as claimed.

The rejections under 35 U.S.C. §103(a) have provided no more motivation than to simply point out the individual words of the Applicant's claims among the references, but without the reason and result as provided in the Applicant's claims and specification, and without reason as to why and how the references could provide the Applicant's invention as claimed. Hindsight cannot be the basis for motivation, which is not sufficient to meet the burden of sustaining a 35 U.S.C. §103(a) rejection.

Thus, claims 1, 16-17 and 18, 33-34 of the present invention are not taught or suggested by Chiang and/or Tu. Combining these references fails to teach or yield the invention as claimed. The combination of these references fails to teach or suggest all the elements of the claims. Further, one of skill in the art would not be motivated to make such a combination. Therefore, the present invention is not obvious in light of any combination of Chiang and/or Tu. Withdrawal of the §103(a) rejection is therefore respectfully requested.

III. Allowable Subject Matter

Claims 7-15 and 24-32 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form, including all of the limitations of the base claim and any intervening claims. The Examiner indicated that claims 7-15 and 24-32 are allowable over the prior art of record, Chiang in view of Tu, because the prior art fails to disclose the formation of an MIM capacitor used in an embedded device wherein the substrate and the layers of the capacitor further include a metal-1 oxide layer, a metal-2 oxide-1 layer, and a copper layer and substrate and layers thereof are subject to a TaN sputter deposition process followed by a photoresist coating and etch operation to form at least one recess in a DRAM cell node.


Applicants are therefore providing new claims 35 and 36 by amendment as indicated herein, which are written forms of claims 7-15. Applicants are also providing new claims 37 and 38, which are written forms of claims 24-32. Applicants therefore believe that claims 35-38 are now in condition for allowance.

IV. Conclusion

In view of the foregoing discussion, Applicants have responded to each and every rejection of the Official Action, and respectfully request that a timely Notice of Allowance be issued. Applicants have clarified the structural distinctions of the present invention and have amended the claims accordingly. Applicants believe that support for such amendments are provided by the Specification. Applicants respectfully submit that the foregoing discussion does not present new issues for consideration and that no new search is necessitated.

Should there be any outstanding matters that need to be resolved in the present application; the Examiner is respectfully requested to contact the undersigned representative to conduct an interview in an effort to expedite prosecution in connection with the present application.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'Randy Tung', is written over a large, loopy circular mark.

Randy Tung
Reg. No. 31,311